

Low Voltage High Performance 1:8 Clock Fanout Buffer

Product Description

The MQC180100 is a member of the Multigig QuietClock™ Series of low noise timing solutions for high speed & accuracy fanout of the reference clock signal.

The MQC180100 is a low skew clock driver that provides a 1:8 fanout ratio with low additive jitter. The eight LVCMOS outputs are buffered from a single input to reduce loading on the preceding driver and provide an efficient and quiet (low noise) clock distribution network. Outputs are designed for 6 inverting and 2 non-inverting signal to minimize switching noise and minimize corruption of the power supply.

Multiple power and ground pins help to reduce noise. Typical applications are clock and signal distribution in WAN/LAN and computer system designs.

The MQC180100 provides clock fanout much like the popular 74FCT3807, with the advantages of improved jitter, lower power consumption and overall improved waveform integrity. A lower power alternative is now available when a fanout of 8 is required.

Features

- 0.18 MICRON CMOS Technology
- $F_{max} = 250\text{MHz}$
- Guaranteed low skew < 150ps (Max.) - same phase
- Very low duty cycle distortion 49/51% (Typ)
- 1:8 fanout ratio
- Fast Edges
- Typical output rise and fall time < 400ps - 10pf load
- 24mA/24mA drive
- Low input capacitance: 4.5pF typical
- Low Voltage Operation
- $V_{DD} = 3.3V \pm 10\%$
- Industrial Temperature range is standard
- -40 to +85 °C
- Available in 20 pin SOIC or SSOP GREEN package



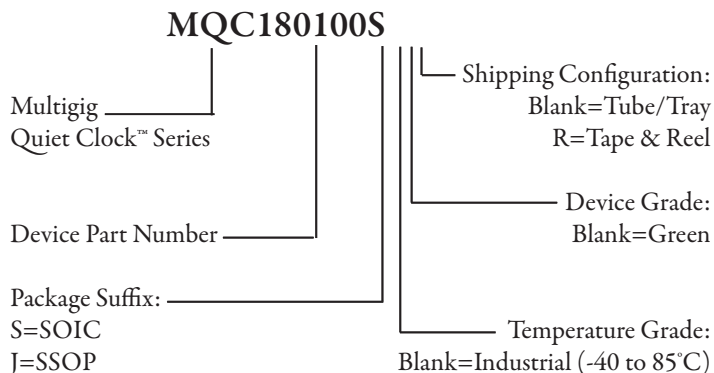
20-Lead SOIC

MQC180100

NC	□ 1	20	□ OUTPUT8
VSS	□ 2	19	□ VSS
OUTPUT1	□ 3	18	□ OUTPUT7
VDD	□ 4	17	□ OUTPUT6
IN	□ 5	16	□ VDD
VSS	□ 6	15	□ OUTPUT5
OUTPUT2	□ 7	14	□ OUTPUT4
NC	□ 8	13	□ VSS
VDD	□ 9	12	□ OUTPUT3
VDD	□ 10	11	□ VSS

**MQC180100 20-Lead SOIC Pinout
(Top View)**

MQC180100 Ordering Information:



MQC180100 Block Diagram

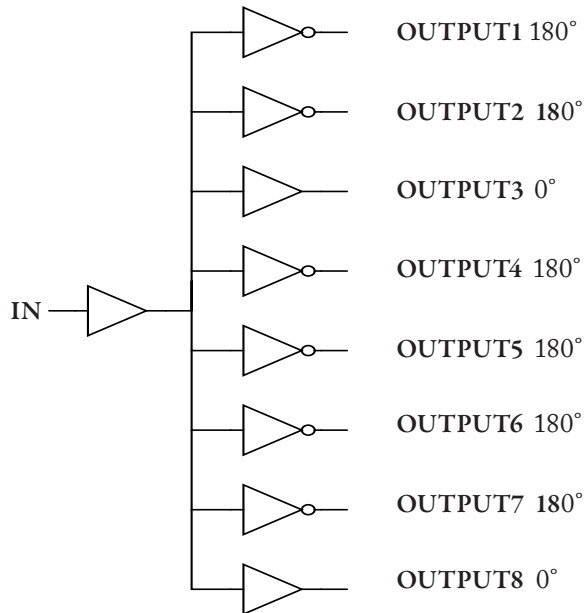


Figure-1

Device Description

The MQC180100, part of the Multigig Quiet Clock Series, provides performance improvements to the clock fanout tree. Additive jitter is reduced, skew is reduced, and duty cycle error has been tightened. 6 outputs are inverting, and 2 are noninverting, to reduce the dI/dt impact on both output waveforms as well as system power supplies. To optimize duty cycle fidelity, the buffers are internally C-coupled, resulting in a 1MHz minimum operating frequency. Internally, devices are individually filtered and bypassed to provide the best possible jitter performance in the presence of noisy power busses. In second source applications, please note the input is not 5 volt tolerant, nor does it have hysteresis.

Absolute Maximum Ratings

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	-0.5 to +4.6	V
V_{IN}	Input Voltage	-0.5 to $V_{DD}+0.5$	V
V_{OUT}	Output Voltage	-0.5 to $V_{DD}+0.5$	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C

NOTE: Exposure to stresses at or beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device and may affect product reliability. These are absolute maximum specifications only, and functional operation of the device at these conditions or any conditions beyond those listed is not implied or recommended.

IC Pinout Description

Pin #	Name	Type	Level	Description
1	NC			No Connect
2	V_{SS}	PWR		
3	OUTPUT1	O	LVC MOS	OUTPUT - 180° to IN
4	V_{DD}	PWR		
5	IN	I	LVC MOS	Input Clock
6	V_{SS}	PWR		
7	OUTPUT2	O	LVC MOS	OUTPUT - 180° to IN
8	NC			No Connect
9	V_{DD}	PWR		
10	V_{DD}	PWR		
11	VSS	PWR		
12	OUTPUT3	O	LVC MOS	OUTPUT - 0° to IN
13	V_{SS}	PWR		
14	OUTPUT4	O	LVC MOS	OUTPUT - 180° to IN
15	OUTPUT5	O	LVC MOS	OUTPUT - 180° to IN
16	V_{DD}	PWR		
17	OUTPUT6	O	LVC MOS	OUTPUT - 180° to IN
18	OUTPUT7	O	LVC MOS	OUTPUT -180° to IN
19	V_{SS}	PWR	LVC MOS	
20	OUTPUT8	PWR	LVC MOS	OUTPUT - 0° to IN

DC Characteristics (VDD = 3.3V +/- 10%, TA = -40°C to 85°C)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{IH}	Input HIGH Level						V
V_{IL}	Input LOW Level						V
I_{IH}	Input HIGH Current	$V_{DD} = \text{Max.}$	$V_I = \text{MAX}$				uA
I_{IL}	Input LOW Current	$V_{DD} = \text{Max.}$	$V_I = 0$				
V_{IK}	Clamp Diode Voltage	$V_{DD} = \text{Min.}, I_{IN} = -18\text{mA}$					
I_{ODH}	Output HIGH Current	$V_{DD} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}$					
I_{ODL}	Output LOW Current	$V_{DD} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}$					
I_{OS}	Short Circuit Current	$V_{DD} = \text{Max.}, V_O = \text{GND}$			35		mA
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{IOH} =$				mA
			$I_{IOH} =$				
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{IOL} =$				mA
			$I_{IOL} =$				

AC Characteristics (VDD = 3.3V +/- 10%, TA = -40°C to 85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay - Low to High	$C_L = 10\text{pF}$ $f \leq 250\text{MHz}$				ns
t_{PHL}	Propagation Delay - High to Low					ns
t_R	Output Rise Time 20%-80%				400	ps
t_F	Output Fall Time 20%-80%				400	ps
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew - Same Phase				150	ps
$t_{SK(OP)}$	Same Device Output Skew - Opposite Phases					ps
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $					ps
$t_{SK(PP)}$	Part-to-Part Skew					ps
f_{IN}	Input Frequency*		1		250	MHz

*Note: Internally C-coupled; No DC operation allowed.

AC Characteristics (VDD = 3.3V +/- 10%, TA = -40°C to 85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay - Low to High	$C_L = 0pF$ $f \leq 250MHz$ $RL = 50ohm \text{ to } V_{dd}/2$		2.5		ns
t_{PHL}	Propagation Delay - High to Low			2.5		ns
t_R	Output Rise Time 20%-80%			215	400	ps
t_F	Output Fall Time 20%-80%			196	400	ps
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew - Same Phase			20	150	ps
$t_{SK(OP)}$	Same Device Output Skew - Opposite Phases			80		ps
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $					ps
$t_{SK(PP)}$	Part-to-Part Skew					ps
f_{IN}	Input Frequency*			1		250

*Note: Internally C-coupled; No DC operation allowed.

Capacitance

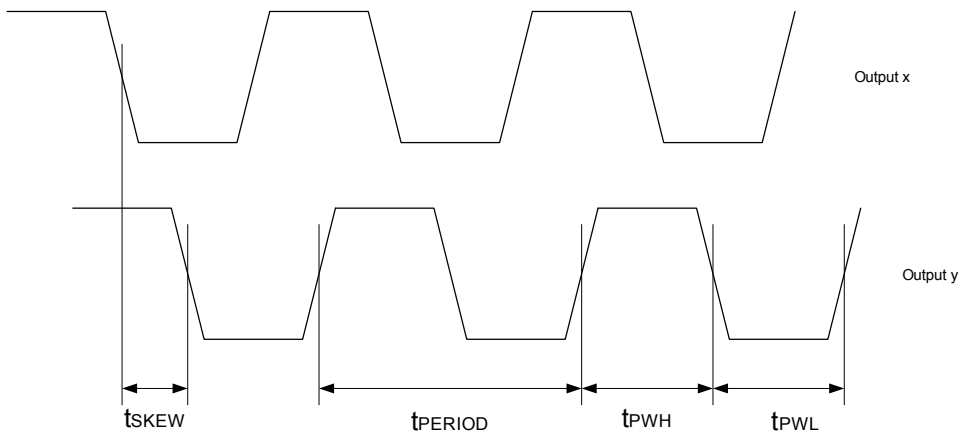
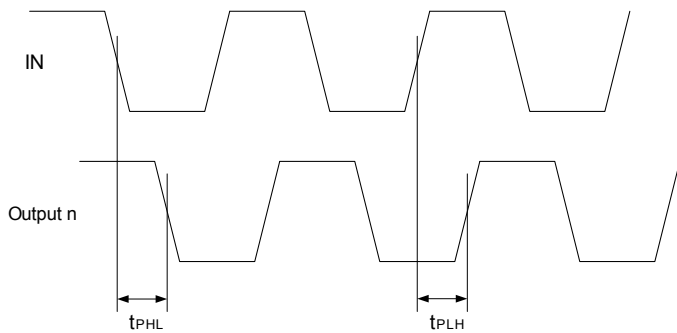
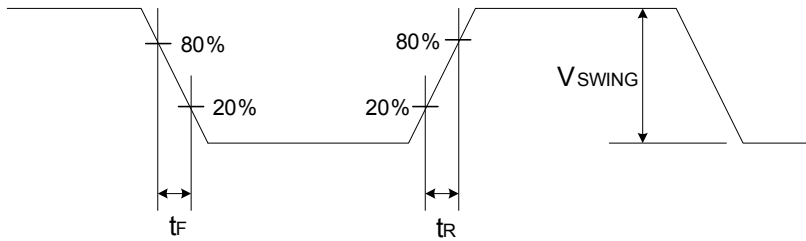
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	3	4.5		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		6		pF

Power

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Total Power Supply Current	$V_{DD} = \text{Max.}$ $C_L = 10pF$ All Outputs Toggling $F_{IN} = 250MHz$		130	226	mA



Switching Waveforms





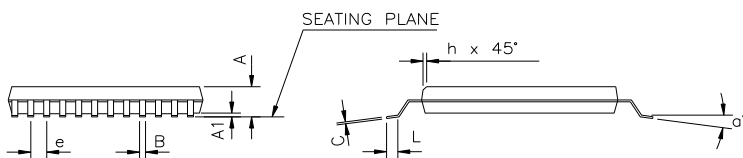
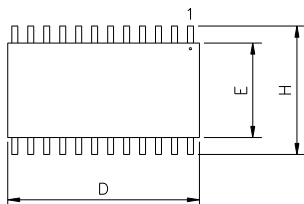
Package Outline Drawing - SOIC

300 MIL SOIC
PLASTIC SMALL OUTLINE GULLWING

PACKAGE INFORMATION

NOTES

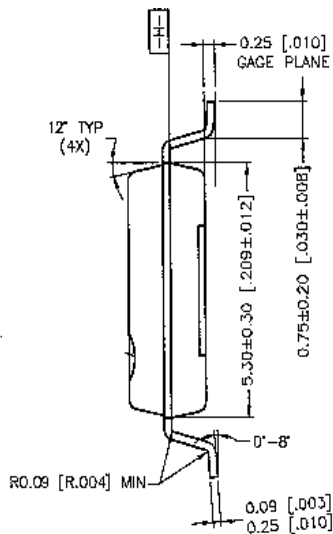
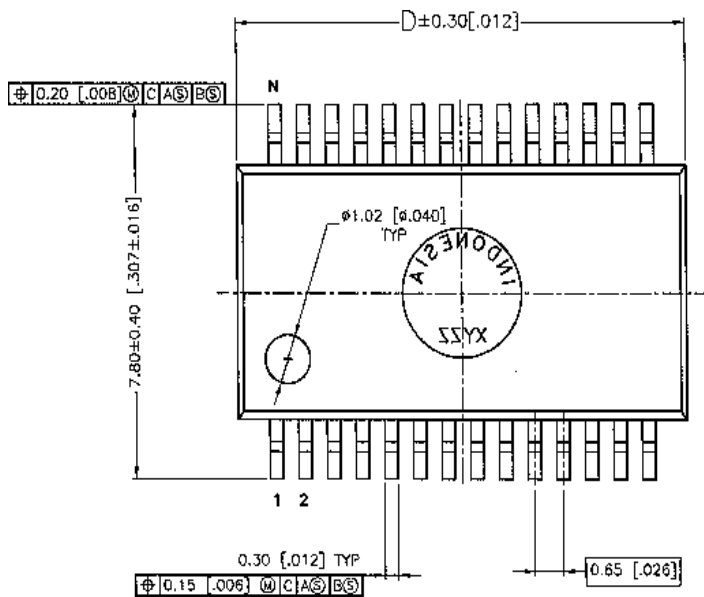
1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. DIMENSIONS ARE GIVEN IN INCHES.
5. LEAD COPLANARITY IS 0.003 INCH MAX.



JEDEC #	MS-013AC	
TYPE	20 LEAD	
SYMBOL	Min	Max
A	0.096	0.104
A1	0.005	0.011
B	0.014	0.019
C	0.009	0.012
D	0.500	0.510
E	0.292	0.299
e	0.050 BSC	
H	0.396	0.416
h	0.010	0.016
L	0.020	0.040
α°	0	8°



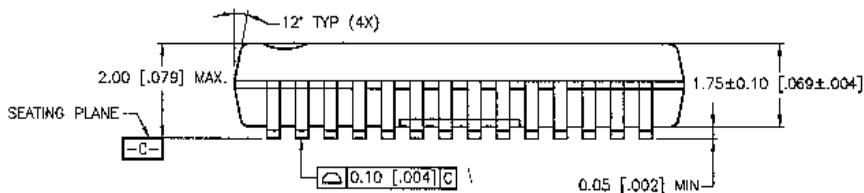
Package Outline Drawing - SSOP



N	D
16	6.20 [0.244]
20	7.20 [0.283]
28	10.20 [0.401]

Notes:

1. Datums -A- and -B- to be determined at Datum Plane -H-
2. Package dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 [0.006] per side.
3. Controlling dimension in mm.
4. Drawing conforms to JEDEC ref. MO-150 rev. B.





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