

High Performance 1:10 Clock Fanout Buffer

Product Description

The MQC1A0110 is a member of the Multigig QuietClock™ Series of low noise timing solutions for high speed & accuracy fanout of the reference clock signal.

The MQC1A0110 is a low skew clock driver that provides a 1:10 fanout ratio with low additive jitter. The 10 LVCMOS outputs are buffered from a single input to reduce loading on the preceding driver and provide an efficient and quiet (low noise) clock distribution network. Outputs are designed for 0 (5 ea) and 180 (5 ea) degree phase relationships in order to minimize simultaneous switching noise, and are optimized for low additive jitter.

Multiple power and ground pins help to reduce noise. Typical applications are clock and signal distribution in WAN/LAN and computer system designs.

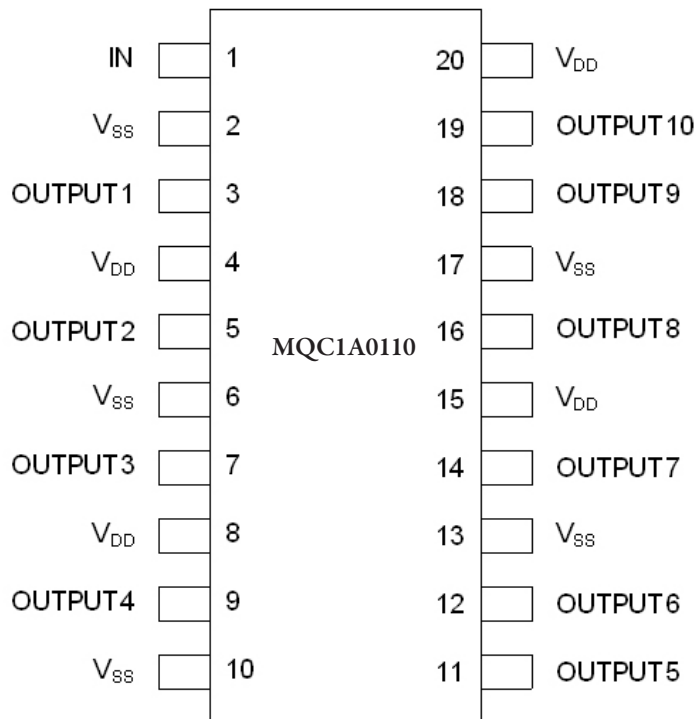
The MQC1A0110 provides an excellent socket alternative for the IDT49/74FCT3807, with improved accuracy, lower power consumption and overall improved waveform integrity, making it an ideal second source.

Features

- 0.18 MICRON CMOS Technology
- $F_{max} = 400\text{MHz}$
- Guaranteed low skew $< 150\text{ps}$ (Max.) - same phase
- Very low duty cycle distortion 48/52% (Typ)
- 1:10 fanout ratio
- Fast Edges
- Typical output rise and fall time $< 400\text{ps}$ - 10pf load
- 24mA/24mA drive
- Low input capacitance: 4.5pF typical
- Low Voltage Operation: $V_{DD} = 3.3\text{V} \pm 10\%$
- Socket Alternative for the 49/74FCT3807xx (IDT, Pericom)
- Industrial Temperature Range
- Green, RoHS Compliant and PFOS Compliant

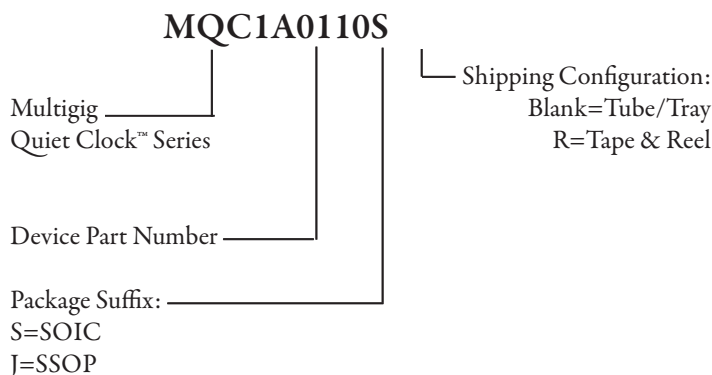


20-Lead SOIC



MQC1A0110 20-Lead SOIC Pinout
(Top View)

MQC1A0110 Ordering Information:



MQC1A0110 Block Diagram

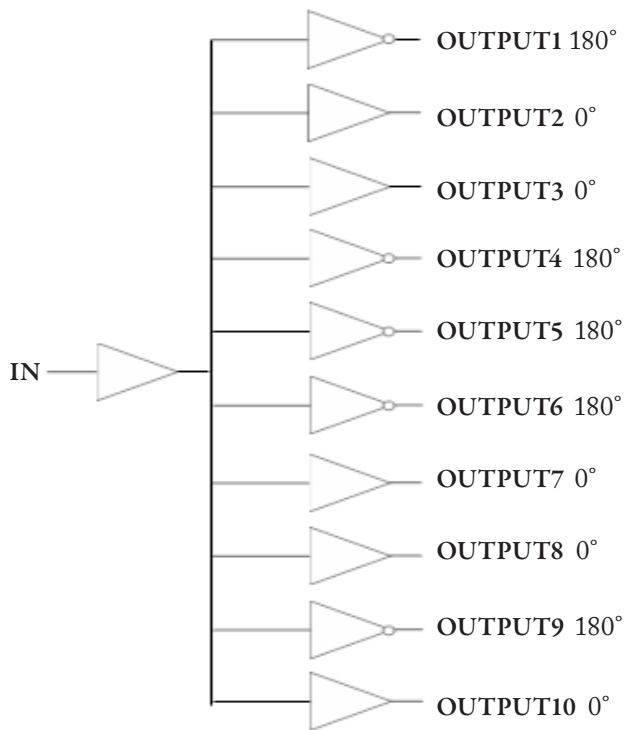


Figure-1

Device Description

The MQC1A0110, part of the Multigig Quiet Clock Series, provides performance improvements to the clock fanout tree. Additive jitter is reduced, skew is reduced, and duty cycle has been tightened. 5 outputs are inverting, and 5 are noninverting, to reduce the dI/dt impact on both output waveforms as well as system power supplies. To optimize duty cycle fidelity, the buffers are internally C-coupled, resulting in a 1MHz minimum operating frequency. Internally, devices are individually filtered and bypassed to provide the best possible jitter performance in the presence of noisy power busses. In second source applications, please note the input is not 5 volt tolerant, nor does it have hysteresis.

Absolute Maximum Ratings

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	-0.5 to +4.6	V
V_{IN}	Input Voltage	-0.5 to $V_{DD}+0.5$	V
V_{OUT}	Output Voltage	-0.5 to $V_{DD}+0.5$	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C

NOTE: Exposure to stresses at or beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device and may affect product reliability. These are absolute maximum specifications only, and functional operation of the device at these conditions or any conditions beyond those listed is not implied or recommended.

IC Pinout Description

Pin #	Name	Type	Level	Description
1	IN	I	LVC MOS	Input Clock
2	V_{SS}	PWR		
3	OUTPUT1	O	LVC MOS	OUTPUT - 180° to IN
4	V_{DD}	PWR		
5	OUTPUT2	O	LVC MOS	OUTPUT - 0° to IN
6	V_{SS}	PWR		
7	OUTPUT3	O	LVC MOS	OUTPUT - 0° to IN
8	V_{DD}	PWR		
9	OUTPUT4	O	LVC MOS	OUTPUT - 180° to IN
10	V_{SS}	PWR		
11	OUTPUT5	O	LVC MOS	OUTPUT - 180° to IN
12	OUTPUT6	O	LVC MOS	OUTPUT - 180° to IN
13	V_{SS}	PWR		
14	OUTPUT7	O	LVC MOS	OUTPUT - 0° to IN
15	V_{DD}	PWR		
16	OUTPUT8	O	LVC MOS	OUTPUT - 0° to IN
17	V_{SS}	PWR		
18	OUTPUT9	O	LVC MOS	OUTPUT -180° to IN
19	OUTPUT10	O	LVC MOS	OUTPUT - 0° to IN
20	V_{DD}	PWR		

DC Characteristics (V_{DD} = 3.3V +/- 10%, T_A = -40°C to 85°C)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V _{IH}	Input HIGH Level						V
V _{IL}	Input LOW Level						V
I _{IH}	Input HIGH Current	V _{DD} = Max.	V _I = MAX				uA
I _{IL}	Input LOW Current	V _{DD} = Max.	V _I = 0				
V _{IK}	Clamp Diode Voltage	V _{DD} = Min, IIN = -18mA					
I _{ODH}	Output HIGH Current	V _{DD} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V					
I _{ODL}	Output LOW Current	V _{DD} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V					
I _{OS}	Short Circuit Current	V _{DD} = Max., V _O = GND			35		mA
V _{OH}	Output HIGH Voltage	V _{DD} = Min. V _{IN} = V _{IH} or V _{IL}	I _{IOH} =				mA
			I _{IOH} =				
V _{OL}	Output LOW Voltage	V _{DD} = Min. V _{IN} = V _{IH} or V _{IL}	I _{IOL} =				mA
			I _{IOL} =				

AC Characteristics (V_{DD} = 3.3V +/- 10%, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PLH}	Propagation Delay	C _L = 10pF F <= 400MHz			TBD	ns
t _{PHL}					TBD	
t _R	Output Rise Time 20%-80%				500	ps
t _F	Output Fall Time 20%-80%				500	ps
t _{SK(O)}	Same Device Output Pin-to-Pin Skew - Same Phase				150	ps
t _{SK(OP)}	Same Device Output Skew - Opposite Phases				TBD	ps
t _{SK(P)}	Pulse Skew t _{PLH} -t _{PHL}				TBD	ps
t _{SK(PP)}	Part-to-Part Skew				TBD	ps
F _{MAX}	Input Frequency				400	MHz
F _{MIN}	Minimum Input Frequency			1		MHz

*Note: Internally C-coupled; No DC operation allowed.

AC Characteristics ($V_{DD} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay - low to high	$C_L = 0pF$ $f \leq 400MHz$ $RL = 50ohm$ to $V_{DD}/2$		2.5	TBD	ns
t_{PHL}	Propagation Delay - high to low			2.5	TBD	ns
t_R	Output Rise Time 20%-80%			215	400	ps
t_F	Output Fall Time 20%-80%			196	400	ps
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew - Same Phase			20	150	ps
$t_{SK(OP)}$	Same Device Output Skew - Opposite Phases			80	170	ps
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $				125	ps
$t_{SK(PP)}$	Part-to-Part Skew				TBD	ps
F_{MAX}	Input Frequency				400	MHz
F_{MIN}	Minimum Input Frequency		1			MHz

*Note: Internally C-coupled; No DC operation allowed.

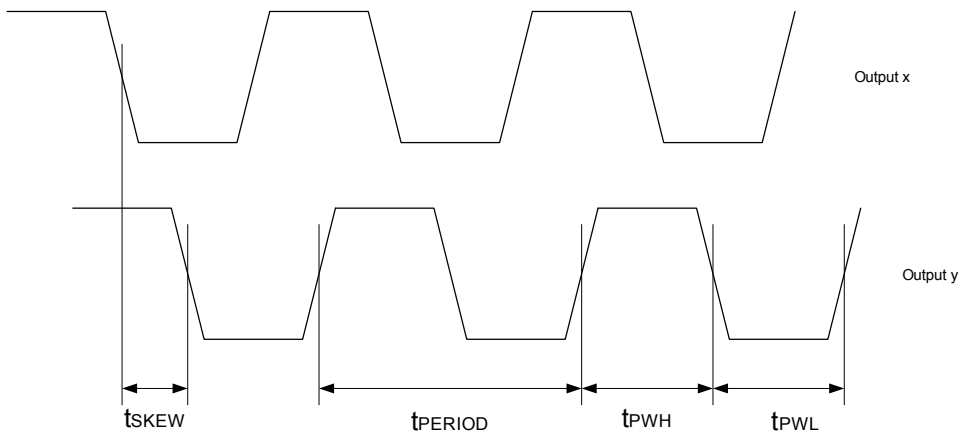
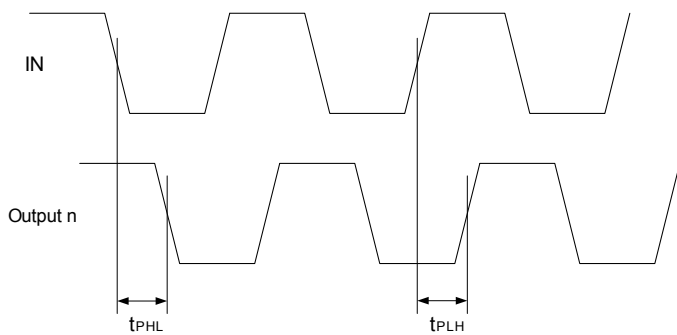
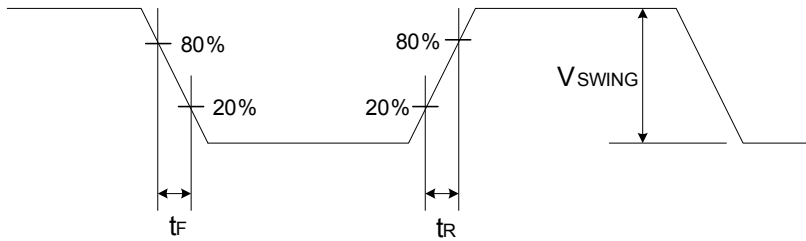
Capacitance

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	3	4.5		pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		6		pF

Power

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_C	Total Power Supply Current	$V_{DD} = Max.$ $C_L = 10pF$ All Outputs Toggling $F_{IN} = 400MHz$		386	525	mA
I_C	Total Power Supply Current	$V_{DD} = Max.$ $R_L = 50ohm$ to $V_{DD}/2$ All Outputs Toggling $F_{IN} = 400MHz$		250	320	mA

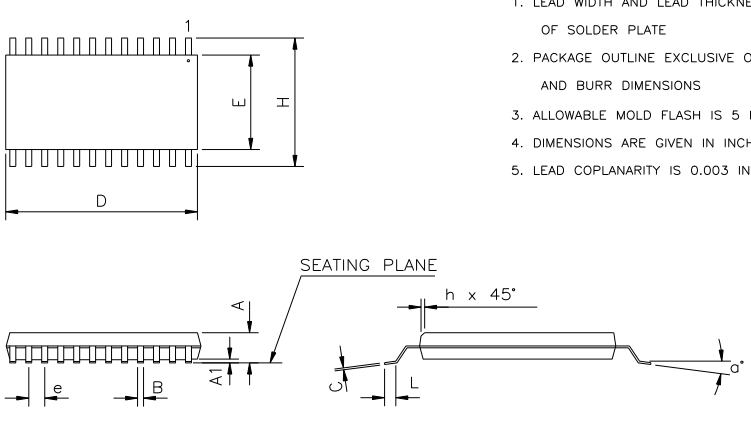
Switching Waveforms



Package Outline Drawing - SOIC

300 MIL SOIC
PLASTIC SMALL OUTLINE GULLWING

PACKAGE INFORMATION

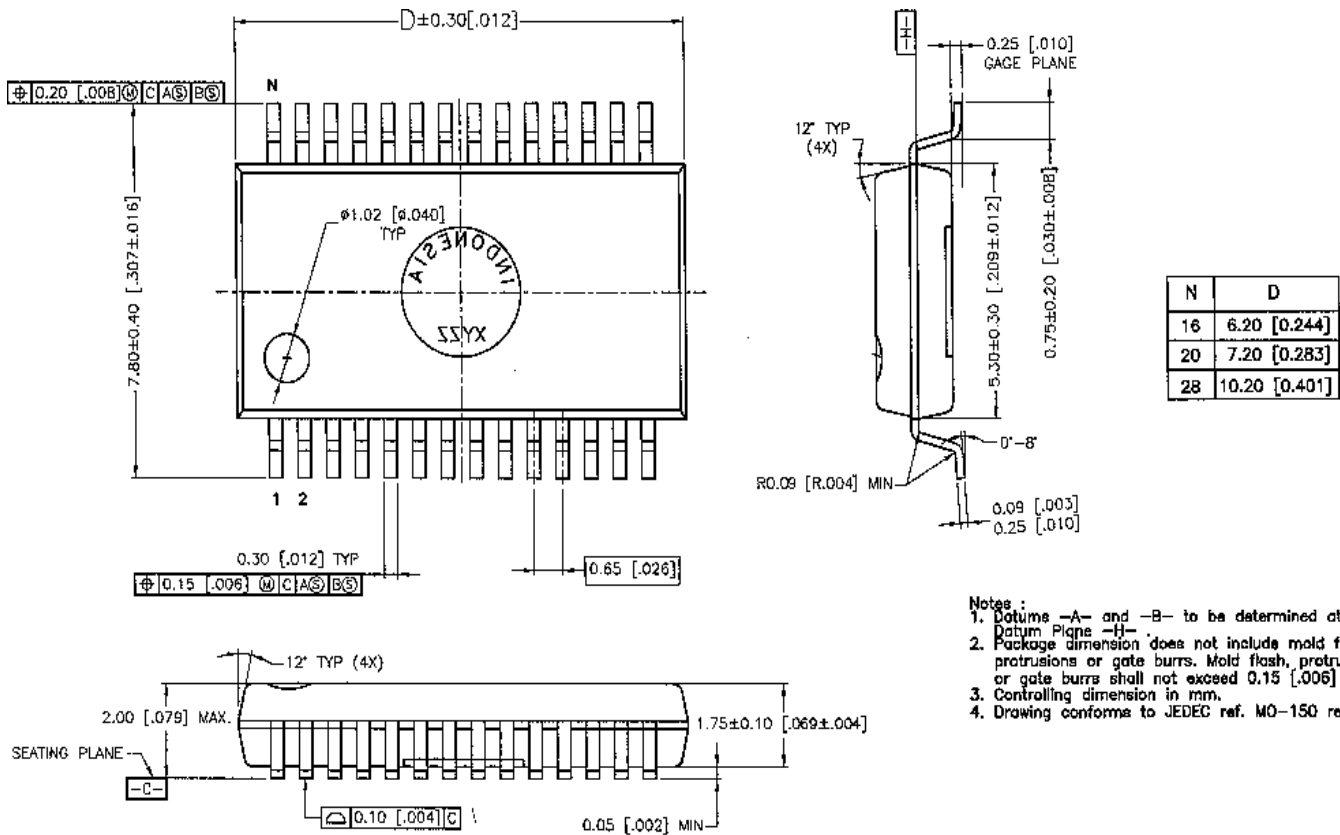


NOTES

1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. DIMENSIONS ARE GIVEN IN INCHES.
5. LEAD COPLANARITY IS 0.003 INCH MAX.

JEDEC #	MS-013AC	
TYPE	20 LEAD	
SYMBOL	Min	Max
A	0.096	0.104
A1	0.005	0.011
B	0.014	0.019
C	0.009	0.012
D	0.500	0.510
E	0.292	0.299
e	0.050 BSC	
H	0.396	0.416
h	0.010	0.016
L	0.020	0.040
α	0	8°

Package Outline Drawing - SSOP



- Notes:
1. Datums -A- and -B- to be determined at Datum Plane -H-
 2. Package dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 [0.006] per side.
 3. Controlling dimension in mm.
 4. Drawing conforms to JEDEC ref. MO-150 rev. B.



Ordering Information

Order Number	Top Marking	Package	Shipping	Temperature
MQC1A0110S	1A0110S	20 Lead SOIC	Tube	-40°C to 85°C
MQC1A0110SR	1A0110S	20 Lead SOIC	Tape & Reel	-40°C to 85°C
MQC1A0110J	1A0110J	20 Lead SSOP	Tube	40°C to 85°C
MQC1A0110JR	1A0110J	20 Lead SSOP	Tape & Reel	40°C to 85°C

Devices are Green, RoHS Compliant and PFOS Compliant.
Lead finish is 100% matte tin.

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