

Low Voltage High Performance Clock Synthesizer

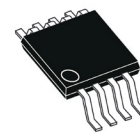
Product Description

The Multigig QuietClock™ synthesizer series were designed with communications standards in mind (Ethernet). The device design for the MQC843022 is optimized for 125MHz using a standard 25MHz fundamental parallel resonant crystal, with unparalleled stability and accuracy over the full operating range, and provides an easy fit for Jitter and Phase Noise standards that require high performance interfaces. The MQC843022 design includes a unique power reduction methodology and along with the Multigig QuietClock™ architecture based upon our proprietary RotaryWave™ technology. This provides a very stable clock with very low noise for optimized performance yielding an overall improved Bit Error Rate (BER) and improved waveform integrity.

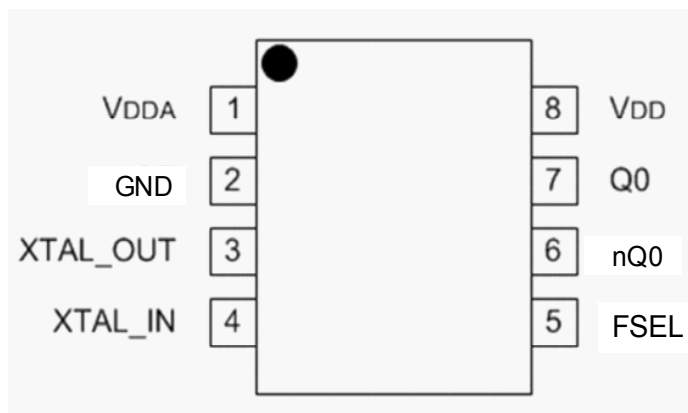
Features

- Generates an optimized 125 MHz LVPECL Output
- Integrated loop filter components
- Operates with either a 3.3 V or 2.5 V supply
- Power consumption is <75mA @ 3.3 V
- Input Frequency: 25 MHz
- Fundamental parallel resonant crystal
- Output Frequency: 125 or 62.5 MHz
- RMS Phase Noise @ 125 MHz versus Frequency offset:

100 Hz:	-110 dBc/Hz
1 kHz:	-127 dBc/Hz
10 kHz:	-132 dBc/Hz
100 kHz:	-129 dBc/Hz
1 MHz:	-142 dBc/Hz
10 MHz:	-152 dBc/Hz
- Available in RoHs or fully Green Compliant packages



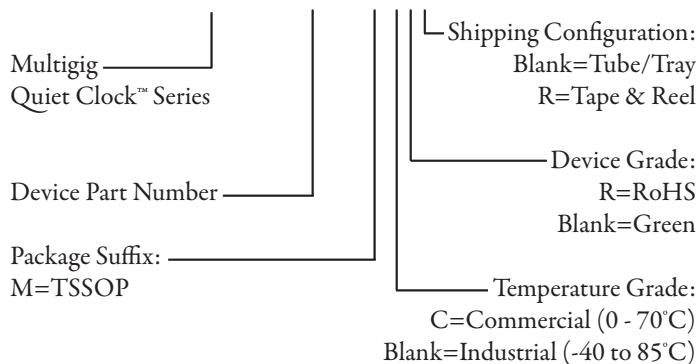
8-Lead TSSOP



MQC843022 8-Lead TSSOP Pinout
(Top View)

MQC843022 Part Number:

MQC843022M



MQC843022 Block Diagram

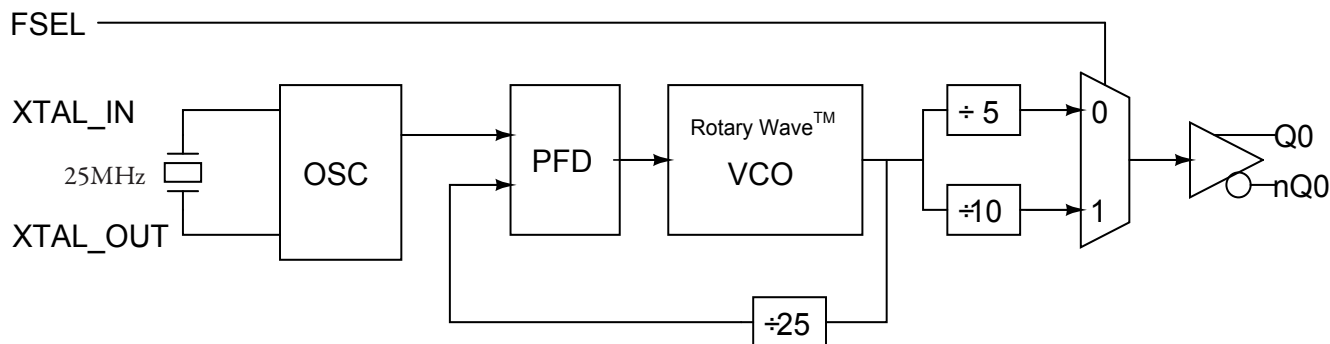


Figure-1

Device Description

Based Upon the unique Multigig Rotary Travelling Wave Oscillator (“RTWO”) synthesizer, the MQC843022 provides a high performance and high accuracy solution for a precision clock source at 125 or at 62.5MHz derived from a low cost 25MHz Xtal. A pair of LVPECL outputs are provided, which should be terminated with 50 ohms to VDD-2.

The design of the MQC843022 consumes very low power in the PLL due to the RTWO technology in the VCO and the associated dividers. The output divider is selectable from div 5 to div 10 via the FSEL pin. The feedback divider is fixed at div 25 providing a selection of 62.5 or 125 MHz. The 62.5 MHz output case leaves a lock spur in-band, resulting in higher jitter. Duty Cycle is inherently improved due to the RTWO technology and guarantees tight control and stability on this critical specification.

The device is fully pin compatible with the ICS/IDT843022 FemtoClock with improved specifications for Duty Cycle, Jitter, Phase Noise, Power Consumption, and noise sensitivity, plus, the MQC843022 will operate at either 3.3V or 2.5V supplies.

Preliminary Information



QuietClock™ Series

MQC843022

IC Pinout Description

Pin #	Name	Type	Level	Description
1	VDDA	P		Analog power
2	GND	P		Ground
3	XTAL OUT	O		Crystal Output
4	XTAL IN	I		Crystal Input
5	FSEL	I	LVC MOS	Pulldown. 0 = 125 MHz, 1 = 62.5 MHz
6	nQ0	O	LVPECL	complementary Q0 output
7	Q0	O	LVPECL	Q0 output
8	V _{DD}	P		Core Power

Absolute Maximum Ratings

Symbol	Characteristics	Min	Max	Unit	Condition
VDD	Supply Voltage		4.6	V	
VIN	Inputs	-0.50	VDD + 0.5	V	
VOUT	Outputs	-0.50	VDD + 0.5	V	
TA	Operating Temperature Range	-40	+85	°C	Industrial
Ts	Storage Temperature Range	-65	+150	°C	

NOTE:

Exposure to stresses at or beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device and may affect product reliability. These are absolute maximum specifications only, and functional operation of the device at these conditions or any conditions beyond those listed is not implied or recommended.

Preliminary Information



QuietClock™ Series

MQC843022

DC Characteristics ($V_{DD} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VDD	Core supply voltage	2.375	2.50	2.625	V	
VDDA	Analog supply voltage	2.375	2.50	2.625	V	
IDD	Core supply current		12	16.3	mA	No load
IDDL	Core plus load current		39		mA	50 ohms to Vdd-2
IDDA	Analog supply current		43	58.2	mA	No load

DC Characteristics ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VDD	Core supply voltage	3.135	3.30	3.465	V	
VDDA	Analog supply voltage	3.135	3.30	3.465	V	
IDD	Core supply current		12	16.3	mA	No load
IDDL	Core plus load current		39		mA	50 ohms to Vdd-2
IDDA	Analog supply current		44	59.8	mA	No load

LVPECL DC Characteristics

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VOH	Output HIGH voltage		Vdd-0.886		V	VDD = 3.3V \pm 5%
VOL	Output LOW voltage		Vdd-1.716		V	VDD = 3.3V \pm 5%

NOTE:
Outputs terminated with 50 Ohms to VDD-2. See Parameter measurements 3.3V load test circuit.

Preliminary Information



QuietClock™ Series

MQC843022

AC Characteristics ($V_{DD} = 2.5V \& 3.3V \pm 5\%$, $T_A = -40^\circ C \text{ to } 85^\circ C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
FOUT	Output frequency		125 62.5		MHz	FSEL=0 FSEL=1
TJIT	RMS phase jitter 125 MHz		186		fs	Integration Range 1.875 - 20 MHz
TJIT	RMS phase jitter 62.5 MHz		1500		fs	Integration Range 1.875 - 20 MHz
TR / TF	Output rise/fall time	250	384	550	ps	20% to 80%
ODC	Output Duty Cycle	48	50	52	%	

3.3V Carrier Frequency, 125MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-110	dBc/Hz
1kHz	-127	dBc/Hz
10kHz	-132	dBc/Hz
100kHz	-129	dBc/Hz
1MHz	-142	dBc/Hz
1.875MHz	-152	dBc/Hz
10MHz	-152	dBc/Hz
20MHz	-151	dBc/Hz

Crystal Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions
Mode of Oscillation	Fundamental Parallel Resonant				
Frequency		25		MHz	
Equivalent Series Resistance (ESR)			50	Ohm	
Shunt capacitor			7	pF	
Drive level			1	mW	

NOTE: Characterized using a 7pF shunt parallel resonant crystal loaded with 20pf.

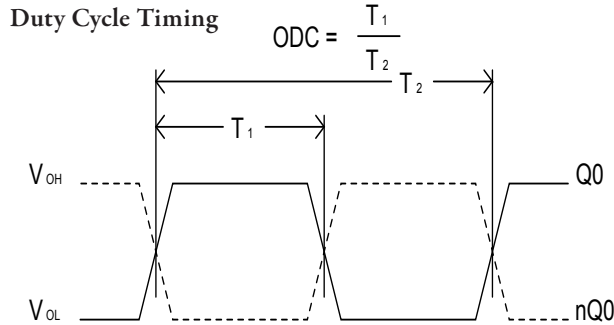
Preliminary Information



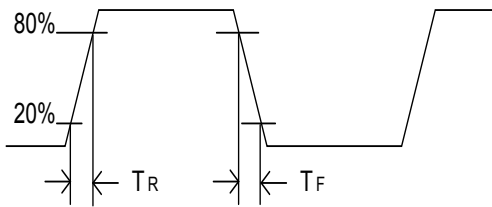
QuietClock™ Series

MQC843022

Switching Waveforms

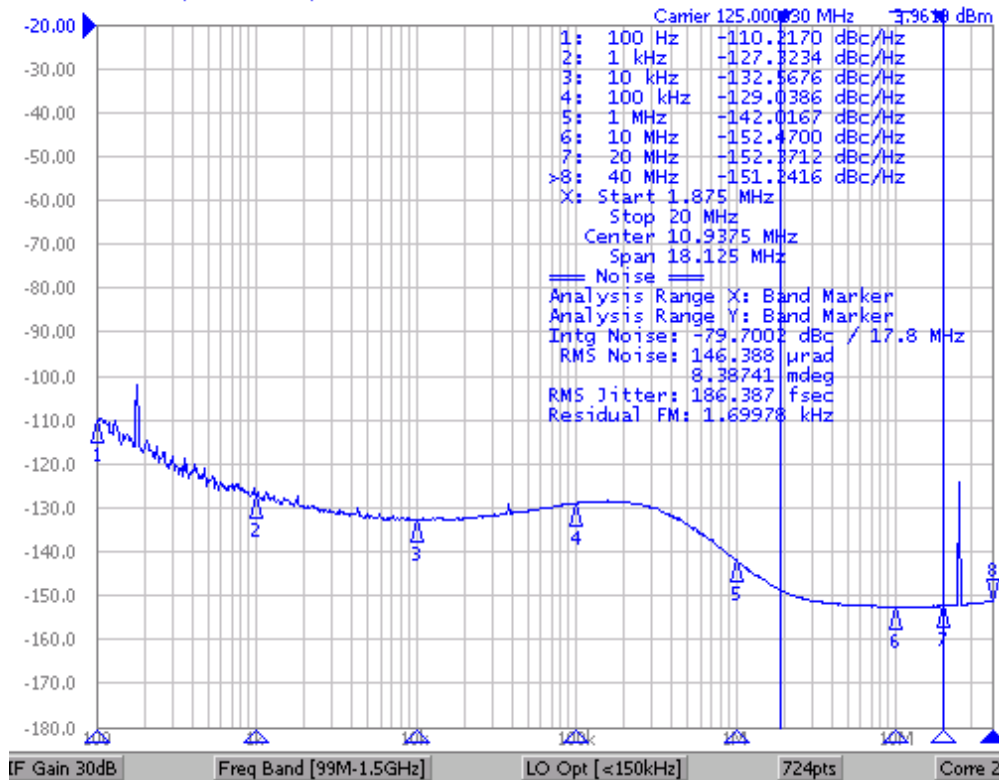


All Outputs Rise/Fall Time

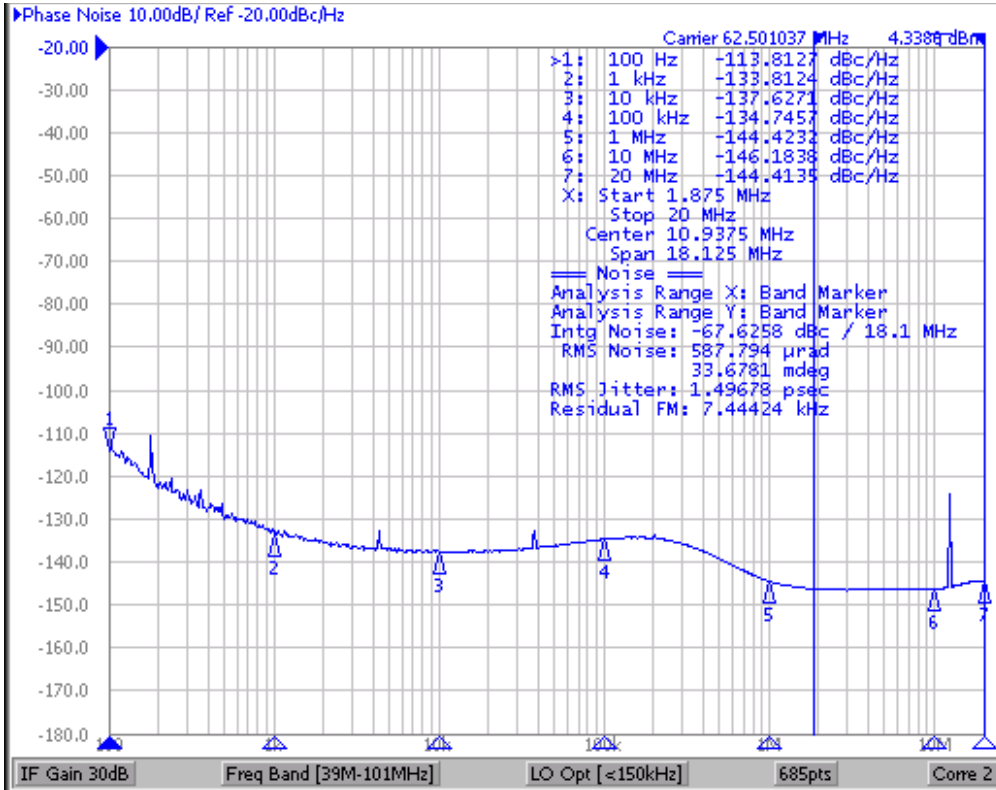


Phase Noise Plot 125 MHz @ 3.3V

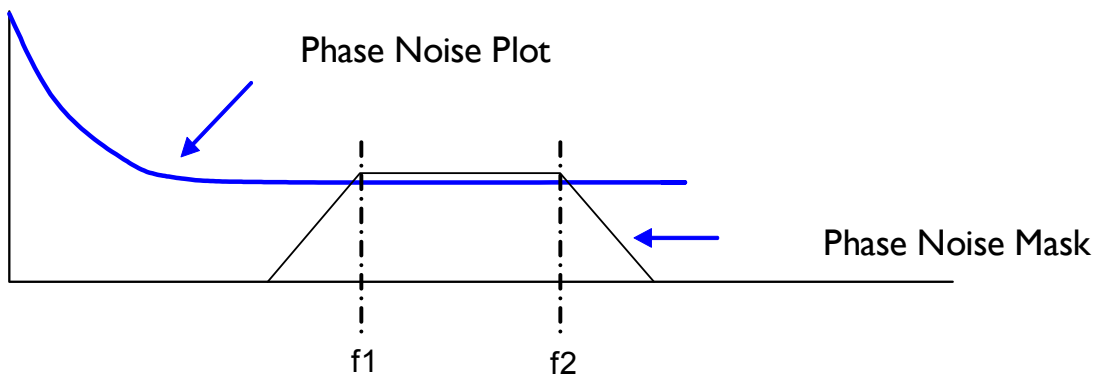
Phase Noise 10.00dB/ Ref -20.00dBc/Hz



Phase Noise Plot 62.5 MHz @ 3.3V

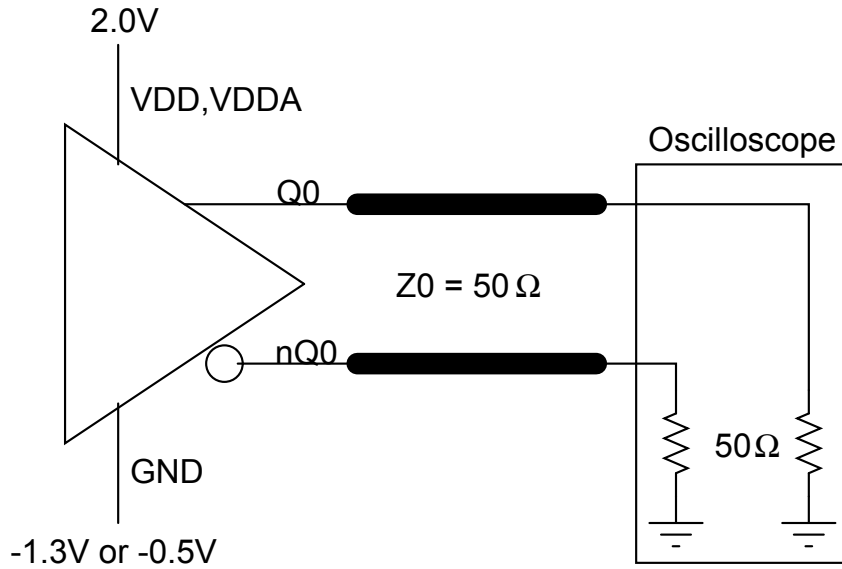


RMS Phase Noise / Jitter



$$\text{RMS Jitter} = \sqrt{\text{Area Under the Phase Noise Plot}}$$

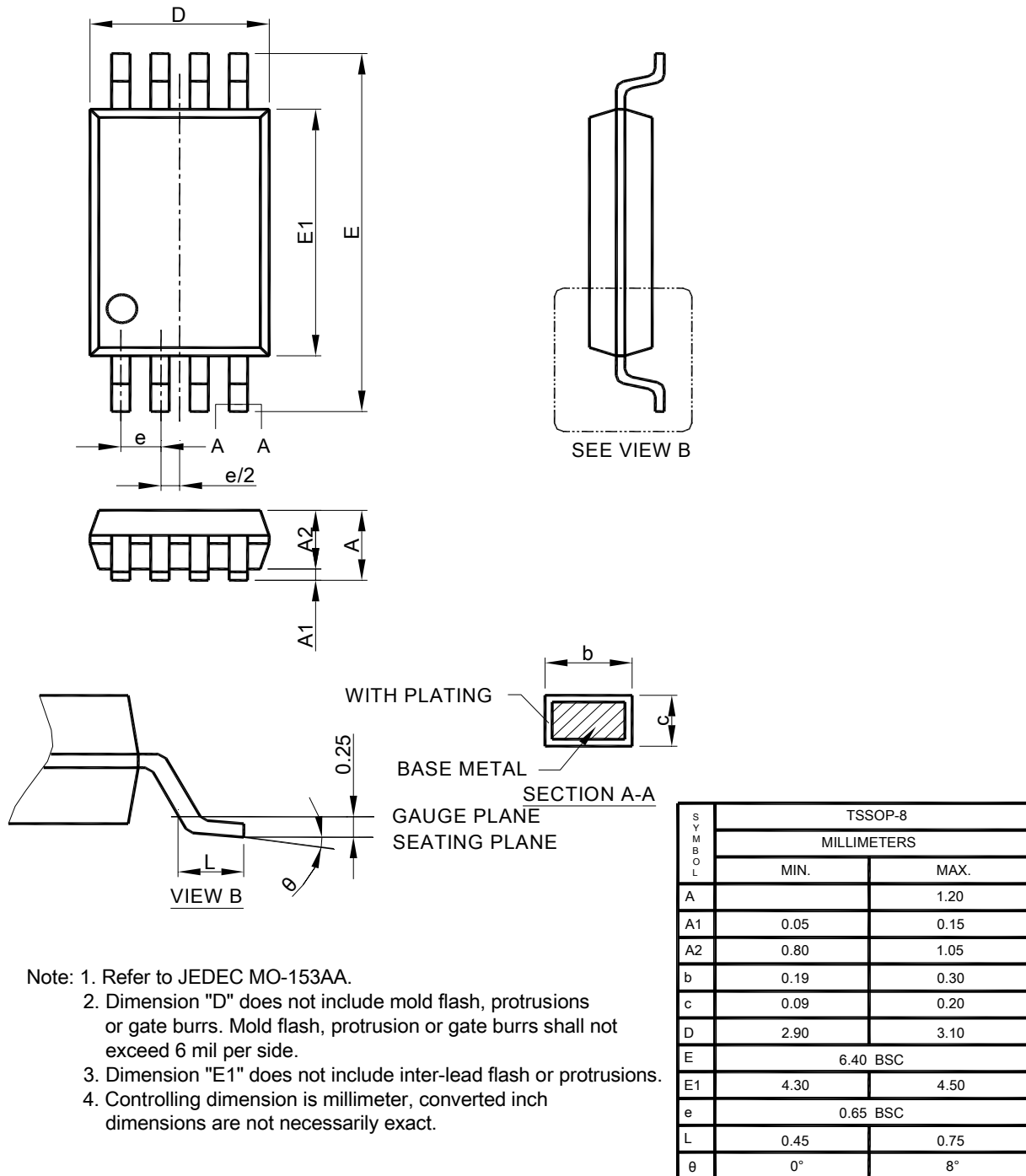
Test Circuit



LVPECL Output Load and Test Circuit

Package Outline Drawing

- TSSOP-8 PACKAGE OUTLINE DRAWING



- Note: 1. Refer to JEDEC MO-153AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E1" does not include inter-lead flash or protrusions.
 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Preliminary Information



QuietClock™ Series

MQC843022

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